

Appl. No. 10/810,023
Amdt. Dated July 24, 2006
Reply to Office Action of June 1, 2006

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REMARKS

Applicants have amended claims 1 and 18, canceled claims 6-17 and 19, and added new claims 20, 21 and 22.

Claim Rejection Under 35 U.S.C. 102

Responsive to the rejection of claims 1-3 and 18 under 35 U.S.C. 102(b) as being anticipated by Jones et al. (U.S. 5,534,743), Applicants have amended claims 1 and 18 and hereby otherwise respectfully traverses this rejection.

Claim 1, as amended, recites in part:

... a shadow mask including a plurality of openings defined therethrough according to a predetermined pattern, the predetermined pattern being in accordance with a pixel pattern of a flat panel display, the shadow mask having an upper surface and a lower surface; and

an insulative layer including a first portion formed on the upper surface of the shadow mask, a plurality of second portions, and a third portion formed on the lower surface of the shadow mask and the second portions disposed in the respective openings and connecting the first portion with the third portion. (Emphasis added.)

Jones et al. fail to disclose or suggest a shadow mask and an insulative layer that includes a first portion formed on an upper surface of the shadow mask, a third portion formed on a lower surface of the shadow mask and a

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plurality of second portions received in respective openings of the shadow mask and connecting the first portion with the third portion, as required by amended claim 1. Specifically, Jones et al. disclose:

Alternating layers of dielectric and insulator material are then deposited on the workpiece structure, including insulator layers 22, of a material such as silicon dioxide, and dielectric layers 24, of a material such as silicon monoxide or aluminum oxide, alternating as shown. On the alternating dielectric/insulator layer stack is deposited a layer 26 of fast etch dielectric material such as alumina, followed by a layer of metal 28, followed in turn by a layer 30 of fast etch dielectric material such as alumina.

Even if the metal layer 28 is considered to be the shadow mask of claim 1, the dielectric layer 30 thereon is continuous across the upper surface metal layer 28, and thus there are no portions of such layer 30 that even extend toward a bottom surface of that metal layer 30. Therefore, claim 1, as amended, is neither taught, disclosed, nor suggested by Jones et al. or any of the other cited references, taken alone or in combination.

Furthermore, the shadow mask and the second portions of the insulative layer of the present invention produce new and unexpected results. A shadow mask used in the device of claim 1 can be made by a known technology in the flat panel display field with a high precision, and the claimed barrier array is convenient and inexpensive to make. In addition, the barrier array of the claim 1, as amended, is disposed between a gate electrode layer and a cathode electrode including a substrate and a plurality of field emitter elements formed on the substrate. The first portion of the insulative layer is disposed on the upper surface of the shadow mask for

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insulating the shadow mask and the gate electrode layer. The third portion of the insulative layer is disposed on the lower surface of the shadow mask for insulating the shadow mask and the substrate. The second portions of the insulative are disposed in the respective openings respectively and connect the first portion with the third portion for insulating the shadow mask and the respective field emitter elements received in the respective openings, thereby aiding uniformity of electron emission from the respective field emitter elements. Therefore, claim 1, as amended, is patentable over Jones et al. under U.S.C. 102 and 103.

Accordingly, claim 1, as amended, is now in condition for allowance, the allowance of which is hereby respectfully requested.

Claims 2 and 3 each are directly dependent from claim 1, and, as such, Applicants submit that claims 2 and 3 should also be allowable.

Claim 18, as amended, recites in part:

... an insulative layer including a first portion formed on the upper surface of the metal plate and a plurality of second portions, the second portions extending from the first portion into the respective openings and formed on inner edges of the metal plate that bound the respective openings. (Emphasis added.)

Jones et al. fail to disclose or suggest an insulative layer configured in the manner provided in claim 18, as amended. As set forth above in the discussion with respect to claim 1, Jones et al. discloses a metal layer 28 and an insulative layer 30 formed on an upper surface of the metal layer 28. Yet,

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no portion of that insulative layer 30 extends into the respective openings and thus onto inner edges of the metal layer 28. Therefore, claim 18, as amended, is not taught or suggested by Jones et al. or any of the other cited references, taken alone or in combination.

Furthermore, the second portions of the insulative layer of the present invention produce new and unexpected results. The barrier array of the present invention is disposed between a gate electrode layer and a cathode electrode including a substrate and a plurality of field emitter elements formed on the substrate. The first portion of the insulative layer is disposed on the upper surface of the metal plate for insulating the metal plate and the gate electrode layer. The second portions of the insulative layer extend from the first portion into the respective openings and are formed on inner edges of the metal plate that bound the respective openings of the metal plate for insulating the metal plate and the respective field emitter elements received in the respective openings, thereby aiding uniform electron emission from the respective field emitter elements. Therefore, claim 18, as amended, is patentable over Jones et al. under U.S.C. 102 and 103.

Accordingly, claim 18, as amended, is now in condition for allowance, the allowance of which is hereby respectfully requested.

Claim Rejection Under 35 U.S.C. 103

Claims 4 and 5 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Jones et al. (U.S. 5,534,743). Applicants submit that

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claims 4 and 5 are each directly dependent from now-allowable claim 1 and, as such, are now in condition for allowance, the allowance of which is hereby respectfully requested.

New Claims

New claims 20, 21 and 22 are each directly dependent from now-allowable claim 18 and are provided to further protect the subject matter of the present invention. Applicants submit that claims 20, 21 and 22 are now in condition for allowance, the allowance of which is hereby respectfully requested.

In view of the foregoing, the present application as defined in the pending claims is considered to be in a condition for allowance, and an action to such effect is earnestly solicited.

Respectfully submitted,
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